REMARKS

In view of the foregoing amendments and following remarks, Applicant respectfully requests reconsideration and withdrawal of the rejections set forth in the above-identified Office Action.

Claims 1, 2, 4, 5, and 9 are pending in the application, with claims 1 and 9 being independent. Claims 1, 2, 4, 5 and 9 have been amended herein.

Initially, it is noted that U.S. Patent No. 6,018,363 has been cited in a rejection under 35 U.S.C. § 103, discussed below. However, that document has not been made of record in this case. Accordingly, Applicant is including that document on a Form PTO-1449 filed with the concurrently-filed Supplemental Information Disclosure Statement in order to make that document of record. It is respectfully requested that the Examiner initial and return a copy of the Form PTO-1449.

Claims 1, 2, 4, 5 and 9 were rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite. Without conceding the propriety of this rejection, Applicant has reworded the language questioned by the Examiner. Reconsideration and withdrawal of the § 112, second paragraph, rejection are requested.

Claims 1, 5 and 9 were rejected under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 6,219,156 (Yoshida, et al.). Claim 2 was rejected under 35 U.S.C. § 103 as being unpatentable over Yoshida, et al. in view of U.S. Patent No. 6,018,363 (Horii). Claims 1 and 4 were rejected under § 103 as being unpatentable over U.S. Patent No. 6,738,093 (Kitagawa, et al.) in view of Yoshida, et al. These rejections are respectfully traversed.

As recited in independent Claim 1, the present invention relates to an image pickup apparatus including an image pickup element, a first memory, an image forming processing circuit, a second memory and an memory control circuit. The first memory stores first image data obtained by the image pickup element. The image forming

processing circuit is adapted to effect image forming processing on the first image data read out of the first memory. The second memory stores second image data subjected to the image forming processing by the image forming processing circuit. The memory control circuit is adapted to carry out in parallel a writing operation of writing the first image data into the first memory and a writing operation of writing the second image data into the second memory. The memory control circuit carries out the parallel writing operations after the first memory stores at least one image frame of the first image data.

As recited in independent Claim 9, the present invention relates to a control method of an image pickup apparatus having an image pickup element, a first memory, a second memory and an image forming processing circuit. The method includes a first writing step of writing first image data obtained by the image pickup element into the first memory and a reading step of reading the first image data already stored in the first memory. The method further includes an image forming processing step for image forming processing on the first image data read out of the first memory in the reading step, and a second writing step of writing second image data subjected to the image forming processing in the image forming processing step into the second memory. The second writing step is performed in parallel with the first writing step after at least one image frame of the first image data is written into the first memory.

Support for the amendments to the claims can be found in the specification at least with respect to the discussion of Figures 11 and 13. Of course, the claims are not intended to be limited in scope to these preferred embodiments.

Yoshida, et al. is directed to an image processing device having an input image memory for temporarily storing digital image data. Reading and compressing of a quantity of the stored image data are performed in parallel with the storing of new image data. As understood by Applicants, image data is divided into a plurality of blocks to write blocks in a first memory, as shown in Figure 5, for example. Compression processing is

performed on that image data on a block basis to write the processed image data into a second memory, such as compressed image memory area 9262. The writing operations of the first and second memories can be performed in parallel as shown in Figure 7, for example. That is, as shown in Figure 7, the parallel writing operation of the first and second memories is performed on a block basis on image data of the same frame. Accordingly, Yoshida, et al. fails to disclose or suggest at least carrying out in parallel a writing operation of writing first image data into a first memory and a writing operation of writing second image data into a second memory, with the parallel writing operations being carried out after the first memory stores at least one image frame of the first image data, as is recited in independent Claim 1. Nor does Yoshida, et al. disclose or suggest at least a second writing step of writing second image data subjected to image forming processing into a second memory, with the second writing step being performed in parallel with a first writing step after at least one image frame of the first image data is written into a first memory, as is recited in independent Claim 9.

Thus, Yoshida, et al. fails to disclose or suggest important features of the present invention recited in the independent claims.

Kitagawa, et al. is directed to a digital imaging apparatus that can store interleaved data from an image sensing section. Figures 4-6 depict timing charts of three embodiments. However, Applicants submit that Kitagawa, et al. fails to disclose or suggest parallel writing operations. For example, in Figures 4 and 5 "WRITE" and "READ" of the two frames are not performed in parallel. As to Figure 6, "WRITE" is performed during the time period T_{32} to T_{33} whereas "READ" is stopped during this period and performed after "WRITE" is completed. Note, for example, column 8, lines 25-40.

Accordingly, Kitagawa, et al. also fails to disclose or suggest at least carrying out in parallel a writing operation of writing first image data into a first memory and a writing operation of writing second image data into a second memory, with the parallel writing operations being carried out after the first memory stores at least one image frame of the first image data, as is recited in independent Claim 1, or a second step of writing second image data subjected to image forming processing into a second memory, with the second writing step being performed in parallel with a first writing step after at least one image frame of first image data is written into the first memory, as is recited in independent Claim 9.

Thus, Kitagawa, et al. fails to disclose or suggest important features of the present invention recited in independent claims.

Even if the plural memory areas of Yoshida, et al. were incorporated into the apparatus of Kitagawa, et al., the resulting combination would not meet the claimed features noted above as being deficient in either citation taken alone.

Horii was cited by the Examiner for teaching a color processing section for carrying out white balance processing. However, Horii is not believed to remedy the deficiencies of the citations noted above with respect to the independent claims.

Accordingly, reconsideration and withdrawal of the §§ 102 and 103 rejections are respectfully requested.

U.S. Patent No. 6,177,956, which is cited in the accompanying Information Disclosure Statement, discusses performing in parallel writing raw image data from an image sensor 24 into a frame buffer 70 and executing processing by a processing unit 54. However, this citation does not disclose or suggest the memory control circuit recited in Claim 1 or the first and second writing steps recited in Claim 9.

For the foregoing reasons, Applicant respectfully submits that the present invention is patentably defined by independent Claims 1 and 9. Dependent Claims 2, 4 and 5 are also allowable, in their own right, for defining features of the present invention in addition to those recited in independent Claim 1. Individual consideration of these dependent claims is requested.

Applicant submits that the present application is in condition for allowance. Favorable reconsideration, withdrawal of the rejections set forth in the above-noted Office Action, and an early Notice of Allowance are requested.

Applicant's undersigned attorney may be reached in our Washington, D.C., office by telephone at (202) 530-1010. All correspondence should continue to be directed to our address below.

Respectfully submitted,

Mark A. Williamson
Attorney for Applicant
Registration No. 33,628

FITZPATRICK, CELLA, HARPER & SCINTO
30 Rockefeller Plaza
New York, New York 10112-3801
Facsimile: (212) 218-2200
MAW/agm

DC_MAIN 222277v1